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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/079,512	02/22/2002	Shunpei Yamazaki	740756-2441	7506

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EXAMINER	
FORDE, REMMON R	
ART UNIT	**PAPER NUMBER**
2826	3

DATE MAILED: 01/15/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/079,512	YAMAZAKI, SHUNPEI	
	Examiner	Art Unit	
	Remmon R. Fordé	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 February 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. *09/440,633* .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 2 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in-
> (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effect under this subsection of a national application published under section 122(b) only if the international application designating the United States was published under Article 21(2)(a) of such treaty in the English language; or
> (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that a patent shall not be deemed filed in the United States for the purposes of this subsection based on the filing of an international application filed under the treaty defined in section 351(a).

Claims 1-30 are rejected under 35 U.S.C. 102(e) as being anticipated by Nakajima et al..

Regarding claims 1 and 4-6, referring to Figures 13 and 14, Nakajima et al. discloses a poly-Si transistor (TFT) to be used in an active matrix type liquid crystal display device (column 1, lines 24-38). The poly-Si transistor (TFT) is provided on a substrate (10) having an insulating surface (i.e. surface of transparent insulating film (11)). In addition, the TFT contains a semiconductor layer consisting of Si:H and having a channel forming region (12), a source region (13), a drain region (14), and at least one impurity region (52) located between the source (13) and the channel region (12); and a gate electrode (18) formed over the semiconductor layer with a gate insulating film (16) interposed therebetween; wherein the impurity region (52) is partially overlapped with a portion of the gate electrode, and wherein the overlapped portion of the gate electrode

has a thinner thickness than that of a portion of the gate electrode above the channel region. (Column 1, line 18 – Column 3, line 20.)

Regarding claim 2, referring to Figures 13 and 14, Nakajima et al. further discloses an angle formed between a side of the gate electrode (18) and the gate insulating film (16) is 30 degrees.

Regarding claim 3, referring to Figures 13 and 14, Nakajima et al. further discloses that the impurity region (52) and the source (13) and the drain (14) regions include one of periodic table group 15 elements (Phosphorous) as an impurity element. (Column 2, lines 10-15.)

Regarding claims 7 and 10-12, referring to Figures 13 and 14, Nakajima et al. discloses a poly-Si transistor (TFT) to be used in an active matrix type liquid crystal display device (column 1, lines 24-38). The poly-Si transistor (TFT) is provided on a substrate (10) having an insulating surface (i.e. surface of transparent insulating film (11)). In addition, the TFT contains a semiconductor layer consisting of Si:H and having a channel forming region (12), a source region (13), a drain region (14), and at least one impurity region (52) located between the source (13) and the channel region (12); and a gate electrode (18) formed over the semiconductor layer with a gate insulating film (16) interposed therebetween; wherein the impurity region (52) is partially overlapped with a portion of the gate electrode, and wherein the portion of the gate electrode overlapped with the impurity region (52) is a tapered portion of the gate electrode. (Column 1, line 18 – Column 3, line 20.)

Regarding claim 8, referring to Figures 13 and 14, Nakajima et al. further discloses that the tapered portion has an angle of 30 degrees between a side of the gate electrode (18) and the gate insulating film (16).

Regarding claim 9, referring to Figures 13 and 14, Nakajima et al. further discloses that the impurity region (52) and the source (13) and the drain (14) regions include one of periodic table group 15 elements (Phosphorous) as an impurity element. (Column 2, lines 10-15.)

Regarding claims 13 and 16-18, referring to Figures 13 and 14, Nakajima et al. discloses a poly-Si transistor (TFT) to be used in an active matrix type liquid crystal display device (column 1, lines 24-38). The poly-Si transistor (TFT) is provided on a substrate (10) having an insulating surface (i.e. surface of transparent insulating film (11)). In addition, the TFT contains a semiconductor layer consisting of Si:H and having a channel forming region (12), a source region (13), a drain region (14), and at least one impurity region (52) located between the source (13) and the channel region (12); and a gate electrode (18) formed over the semiconductor layer with a gate insulating film (16) interposed therebetween; wherein the impurity region (52) comprises a first portion overlapped with a portion of the gate electrode and a second portion that does not overlapped with the gate electrode, and wherein the portion of the gate electrode overlapped with the first portion has a thinner thickness than that of a portion of the gate electrode above the channel region. (Column 1, line 18 – Column 3, line 20.)

Regarding claim 14, referring to Figures 13 and 14, Nakajima et al. further discloses an angle formed between a side of the gate electrode (18) and the gate insulating film (16) is 30 degrees.

Regarding claim 15, referring to Figures 13 and 14, Nakajima et al. further discloses that the impurity region (52) and the source (13) and drain (14) regions include one of periodic table group 15 elements (Phosphorous) as an impurity element. (Column 2, lines 10-15.)

Regarding claims 19 and 22-24, referring to Figures 13 and 14, Nakajima et al. discloses a poly-Si transistor (TFT) to be used in an active matrix type liquid crystal display device (column 1, lines 24-38). The poly-Si transistor (TFT) is provided on a substrate (10) having an insulating surface (i.e. surface of transparent insulating film (11)). In addition, the TFT contains a semiconductor layer consisting of Si:H and having a channel forming region (12), a source region (13), a drain region (14), and at least one impurity region (52) located between the source (13) and the channel region (12); and a gate electrode (18) formed over the semiconductor layer with a gate insulating film (16) interposed therebetween; wherein the impurity region (52) comprises a first portion overlapped with a portion of the gate electrode and a second portion that does not overlapped with the gate electrode, and wherein the portion of the gate electrode overlapped with the first impurity region is a tapered portion of the gate electrode. (Column 1, line 18 – Column 3, line 20.)

Regarding claim 20, referring to Figures 13 and 14, Nakajima et al. further discloses that the tapered portion has an angle of 30 degrees between a side of the gate electrode and the gate insulating film.

Regarding claim 21, referring to Figures 13 and 14, Nakajima et al. further discloses that the impurity region and the source and drain regions include one of periodic table group 15 (Phosphorous) as an impurity element. (Column 2, lines 10-15.)

Regarding claims 25 and 28-30, referring to Figures 13 and 14, Nakajima et al. discloses a poly-Si transistor (TFT) to be used in an active matrix type liquid crystal display device (column 1, lines 24-38). The poly-Si transistor (TFT) is provided on a substrate (10) having an insulating surface (i.e. surface of transparent insulating film (11)). In addition, the TFT contains a semiconductor layer consisting of Si:H and having a channel forming region (12), a source region (13), a drain region (14), and at least one impurity region (52) located between the source (13) and the channel region (12); and a gate electrode (18) formed over the semiconductor layer with a gate insulating film (16) interposed therebetween; wherein the impurity region (52) comprises a first portion overlapped with a portion of the gate electrode and a second portion that does not overlapped with the gate electrode, and wherein a impurity concentration of the first portion decreases in proportion to a distance from the one of the source and drain regions. (Column 1, line 18 – Column 3, line 20.)

Regarding claim 26, referring to Figures 13 and 14, Nakajima et al. further discloses an angle formed between a side of the gate electrode and the gate insulating film is 30 degrees.

Regarding claim 27, referring to Figures 13 and 14, Nakajima et al. further discloses that the impurity region and the source and drain regions include one of periodic table group 15 elements (Phosphorous) as an impurity element. (Column 2, lines 10-15.)

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Remmon R. Fordé whose telephone number is (703) 305-4533. The examiner can normally be reached on Monday-Friday (8:00-4:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J. Flynn can be reached on (703) 308-6601. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-5841 for regular communications and (703) 308-5841 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Remmon R. Fordé
January 12, 2003

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